Exhibit I

Lu 7,437,583 Applied to Representative Renesas Components and Infotainment Systems and Automobiles Incorporating Those Components

This claim chart compares independent claims 17 and 25 of U.S. Patent No. 7,437,583 ("the Lu '583 patent") to Renesas's R-Car H3 system on a chip ("SoC").

On information and belief, Renesas's R-Car H3 SoC is representative of other Renesas infotainment and high-end car infotainment system SoCs having similar functionality ("Accused Renesas Infotainment SoCs"), including, and without limitation, the Renesas R-Car H2 and the Renesas R-Mobile A1. *See* Declaration of Prof. Bruce McNair ("Ex. 89, McNair Decl.") ¶¶ 12-16.

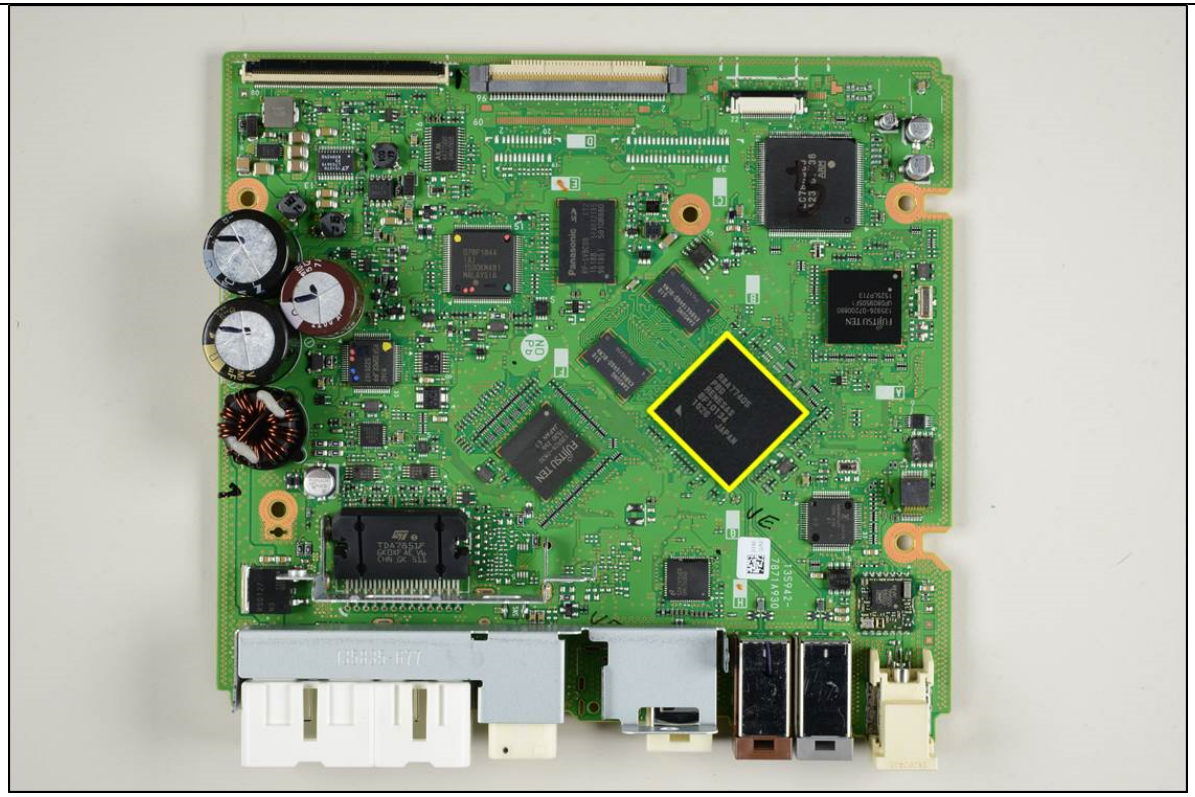
The R-Car H2 SoC is incorporated in downstream products, including without limitation, Panasonic head units, such as Ser No. 112905, that form Accused Toyota Navigation units, including Camry Navigation System with WiFi Hotspot (86840-06011).

The R-Mobile A1 SoC is incorporated in downstream products, including without limitation, at least Denso Ten, formerly Fujitsu Ten, head units, such as Ser. Nos. MMA00002, MM910406, and MM100046, which are incorporated in Accused Toyota Navigation units, including Camry Receiver (86804-06180), Corolla Nav System Kit (86804-02070), and Camry Navigation System Receiver (86804-06100).

On information and belief, the Accused Renesas Infotainment SoCs, and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs, infringe directly, indirectly, and/or under the doctrine of equivalents at least claims 17 and 25 of the Lu '583 patent.

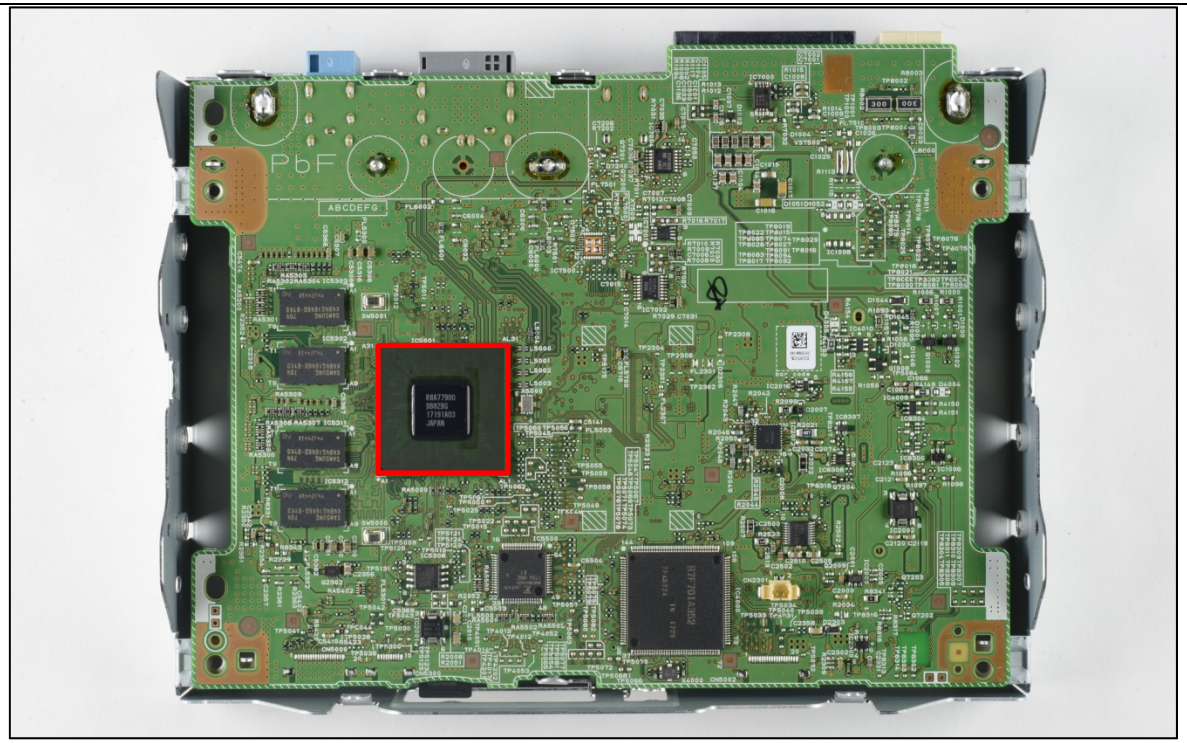
Claims - U.S. Patent No. 7,437,583 (Lu)	**Application of Claim Language to Accused Products**
Claim 17	
A system for distributing clock signals within an electronic device, the system comprising:	To the extent that the preamble is deemed limiting, the Accused Renesas SoCs and downstream products include a system for distributing clock signals within an electronic device. At least the Fujitsu Ten (MM910406) head unit, which is included in at least the Toyota Corolla Navigation System Kit (26187), includes a Renesas R-Mobile A1 SoC (highlighted in yellow).

	 TOYOTA 86804-02070 FUJITSU TEN 139000-0690B101 ASSEMBLED IN MEXICO MM910406 MANUFACTURER FUJITSU TEN LIMITED ADDRESS 2-28, Gosho-dori 1-chome Hyogo-ku, Kobe 652-8510, JAPAN MANUFACTURED September 2015 Complies with 21 CFR Chapter 1, Subchapter J. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. HD Radio Technology manufactured under license from iBiquity Digital Corporation. U.S. and Foreign Patents. HD Radio™ and the HD, HD Radio, and "Arc" logos are proprietary trademarks of iBiquity Digital Corp. AM 530 to 1710kHz FM 87.75 to 107.9MHz FCC ID: BABFT0044C IC: 2024B-FT0044C Model: FT0044C RCPFUFT12-1493 TYPE: FT0044D microSDHC Logo is a trademark of SD-3C, LLC. MM910406 86804-02070



At least the Panasonic (AT1604) head unit, which is included in at least the Toyota Camry Navigation System (301378), includes a Renesas R-Car H2 SoC (highlighted in red).

	 Model No. 86840-06011 Ref. No. CN-SS87N0*XA Set No. AT1604 DC 12V Negative Ground Panasonic Automotive Systems de Mexico S.A. de C.V. Serial No. 112905



The Renesas R-Car H3 SoC includes a system for distributing clock signals within an electronic device.

- Low power dissipation
  Dynamically disables the clocks for the entire VCP4.
  Dynamically disables the clocks for individual submodules.

Ex. 68 – Renesas R-Car H3/M3 Device Manual at 1-11.

VSP2 can stop its operating clock for reducing power consumption.

Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.

<table>
<tr><td></td><td>
Table 17.3 Connected Modules
<table>
<tr><th>Module name</th><th>Connected module name</th><th>Function of connected module</th></tr>
<tr><td rowspan="5">SYS-DMAC</td><td>CPG</td><td>Output clocks</td></tr>
<tr><td>Module Standby</td><td>Control to stop clocks</td></tr>
<tr><td>Software Reset</td><td>Execute software reset</td></tr>
<tr><td>INTC-SYS, INTC-RT</td><td>Control to interrupt</td></tr>
<tr><td>MFI</td><td>Secure function</td></tr>
</table>
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-30.
</td></tr>
<tr><td>at least one processor that determines a status of at least one gate that controls flow of a clock signal to at least one device coupled to said at least one gate; and</td><td>The Renesas R-Car H3’s system for distributing clock signals includes at least one processor that determines a status of at least one gate that controls flow of a clock signal to at least one device coupled to said at least one gate.

For example, the R-Car H3 includes a video signal processor (“VSP2”) that determines a status of at least one gate that controls the flow of a clock signal to the VSP2 by checking the following registers: VI6_CLK_CTRL0, VI6_CLK_CTRL1, VI6_CLK_DCSWT, VI6_CLK_DCSM0, VI6_CLK_DCSM1. By observing the register settings, the VSP2 can determine if the clock stop function is disable, which indicates that the clock gate is not gated.</td></tr>
</table>

	VSP2 can stop its operating clock for reducing power consumption. To enable clock stop function, set following registers: ● VI6_CLK_CTRL0 = H'00000000 ● VI6_CLK_CTRL1 = H'00000000 ● VI6_CLK_DCSWT = H'00000808 ● VI6_CLK_DCSM0 = H'00000000 ● VI6_CLK_DCSM1 = H'00000000. To disable clock stop function, set following registers: ● VI6_CLK_CTRL0 = H'10010F1F ● VI6_CLK_CTRL1 = H'FF00FFFF ● VI6_CLK_DCSWT = H'00130808 ● VI6_CLK_DCSM0 = H'1FFF0F1F VI6_CLK_DCSM1 = H'FF00FFFF Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.
said at least one processor controls said at least one gate based on said determined status.	The Renesas R-Car H3's at least one processor controls said at least one gate based on said determined status. For example, the R-Car H3's VSP2 controls the gate based on the status of the following registers: VI6_CLK_CTRL0, VI6_CLK_CTRL1, VI6_CLK_DCSWT, VI6_CLK_DCSM0, VI6_CLK_DCSM1. If the clock stop function is disabled, then the processor controls the clock gates by keeping the clock gates un-gated. If the clock stop function is enabled, then the processor can clock gate the gates to the VSP2.

<table>
<tr><td></td><td>
VSP2 can stop its operating clock for reducing power consumption.
To enable clock stop function, set following registers:
● VI6_CLK_CTRL0 = H'00000000
● VI6_CLK_CTRL1 = H'00000000
● VI6_CLK_DCSWT = H'00000808
● VI6_CLK_DCSM0 = H'00000000
● VI6_CLK_DCSM1 = H'00000000.
To disable clock stop function, set following registers:
● VI6_CLK_CTRL0 = H'10010F1F
● VI6_CLK_CTRL1 = H'FF00FFFF
● VI6_CLK_DCSWT = H'00130808
● VI6_CLK_DCSM0 = H'1FFF0F1F
VI6_CLK_DCSM1 = H'FF00FFFF
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.
</td></tr>
<tr><td>Claim 25</td><td></td></tr>
<tr><td>A system for distributing clock signals within an electronic device, the system comprising:</td><td>
The Renesas R-Car H3 SoC includes a system for distributing clock signals within an electronic device.
• Low power dissipation
Dynamically disables the clocks for the entire VCP4.
Dynamically disables the clocks for individual submodules.
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 1-11.
VSP2 can stop its operating clock for reducing power consumption.
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.
</td></tr>
</table>

<table>
<tr><td></td><td>
Table 17.3 Connected Modules
<table>
<tr><th>Module name</th><th>Connected module name</th><th>Function of connected module</th></tr>
<tr><td rowspan="5">SYS-DMAC</td><td>CPG</td><td>Output clocks</td></tr>
<tr><td>Module Standby</td><td>Control to stop clocks</td></tr>
<tr><td>Software Reset</td><td>Execute software reset</td></tr>
<tr><td>INTC-SYS, INTC-RT</td><td>Control to interrupt</td></tr>
<tr><td>MFI</td><td>Secure function</td></tr>
</table>
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-30.
</td></tr>
<tr><td>a clock tree having a plurality of gates;</td><td>
The Renesas R-Car H3 includes a clock tree having a plurality of clock gates.

For example, the R-Car H3 includes clock gates for individual submodules in the video codec processor (“VCP4”) and the entire VCP4 and VSP2.

• Low power dissipation
Dynamically disables the clocks for the entire VCP4.
Dynamically disables the clocks for individual submodules.
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 1-11.

VSP2 can stop its operating clock for reducing power consumption.
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.

Table 17.3 Connected Modules
<table>
<tr><th>Module name</th><th>Connected module name</th><th>Function of connected module</th></tr>
<tr><td rowspan="5">SYS-DMAC</td><td>CPG</td><td>Output clocks</td></tr>
<tr><td>Module Standby</td><td>Control to stop clocks</td></tr>
<tr><td>Software Reset</td><td>Execute software reset</td></tr>
<tr><td>INTC-SYS, INTC-RT</td><td>Control to interrupt</td></tr>
<tr><td>MFI</td><td>Secure function</td></tr>
</table>
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-30.
</td></tr>
<tr><td>a hardware control</td><td>The Renesas R-Car H3 includes a hardware control logic block coupled to said clock tree that controls at</td></tr>
</table>

<table>
<tr><td>logic block coupled to said clock tree that controls at least a portion of said plurality of gates;</td><td>least a portion of said plurality of gates.

While the R-Car H3 Device Manual is silent as to how the clock gates are controlled, on SoCs such as the R-Car H3, it is expected that the at least some of the clock gates are controlled by a hardware control block. Ex. 89, McNair Decl. ¶ 17.

Therefore, on information and belief, the R-Car H3 SoC includes a hardware control logic block coupled to said clock tree that controls at least a portion of said plurality of gates. Ex. 89, McNair Decl. ¶ 17.</td></tr>
<tr><td>at least one register that is controlled by a clock tree driver; and</td><td>The Renesas R-Car H3 includes at least one register that is controlled by a clock tree driver.

While the R-Car H3 Device Manual is silent as to how the clock gates are controlled, at least the VSP2 includes registers that enable or disable clock tree functionality. Upon information and belief, these registers would be controlled by clock tree driver software running on a processor. Ex. 89, McNair Decl. ¶ 18.

VSP2 can stop its operating clock for reducing power consumption.
To enable clock stop function, set following registers:
● VI6_CLK_CTRL0 = H’00000000
● VI6_CLK_CTRL1 = H’00000000
● VI6_CLK_DCSWT = H’00000808
● VI6_CLK_DCSM0 = H’00000000
● VI6_CLK_DCSM1 = H’00000000.
To disable clock stop function, set following registers:
● VI6_CLK_CTRL0 = H’10010F1F
● VI6_CLK_CTRL1 = H’FF00FFFF
● VI6_CLK_DCSWT = H’00130808
● VI6_CLK_DCSM0 = H’1FFF0F1F
VI6_CLK_DCSM1 = H’FF00FFFF</td></tr>
</table>

<table>
<tr><td></td><td>Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.

Therefore, on information and belief, the R-Car H3 SoC includes at least one register that is controlled by a clock tree driver. Ex. 89, McNair Decl. ¶ 18.</td></tr>
<tr><td>at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block.</td><td>The Renesas R-Car H3 includes at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block.

While the R-Car H3 Device Manual is silent as to how the clock gates are controlled, at least the VSP2 is a processor that overwrites a status of at least a portion of gates by enabling and disabling the clock stop function. Upon information and belief, at least a portion the gates are controlled by the hardware control logic block. By disabling the clock stop function, gated clocks have their status overwritten to be non-gated clocks. By enabling the clock stop function, non-gated clocks have their status overwritten to allow for clock gating. Ex. 89, McNair Decl. ¶ 19.

VSP2 can stop its operating clock for reducing power consumption.
To enable clock stop function, set following registers:
● VI6_CLK_CTRL0 = H’00000000
● VI6_CLK_CTRL1 = H’00000000
● VI6_CLK_DCSWT = H’00000808
● VI6_CLK_DCSM0 = H’00000000
● VI6_CLK_DCSM1 = H’00000000.
To disable clock stop function, set following registers:
● VI6_CLK_CTRL0 = H’10010F1F
● VI6_CLK_CTRL1 = H’FF00FFFF
● VI6_CLK_DCSWT = H’00130808
● VI6_CLK_DCSM0 = H’1FFF0F1F
VI6_CLK_DCSM1 = H’FF00FFFF
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-41.</td></tr>
</table>

	Therefore, on information and belief, the R-Car H3 SoC includes at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block. Ex. 89, McNair Decl. ¶ 19.